Trends and Challenges in Wireless SOC Design

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Lausanne Mar-22-2013

Agenda

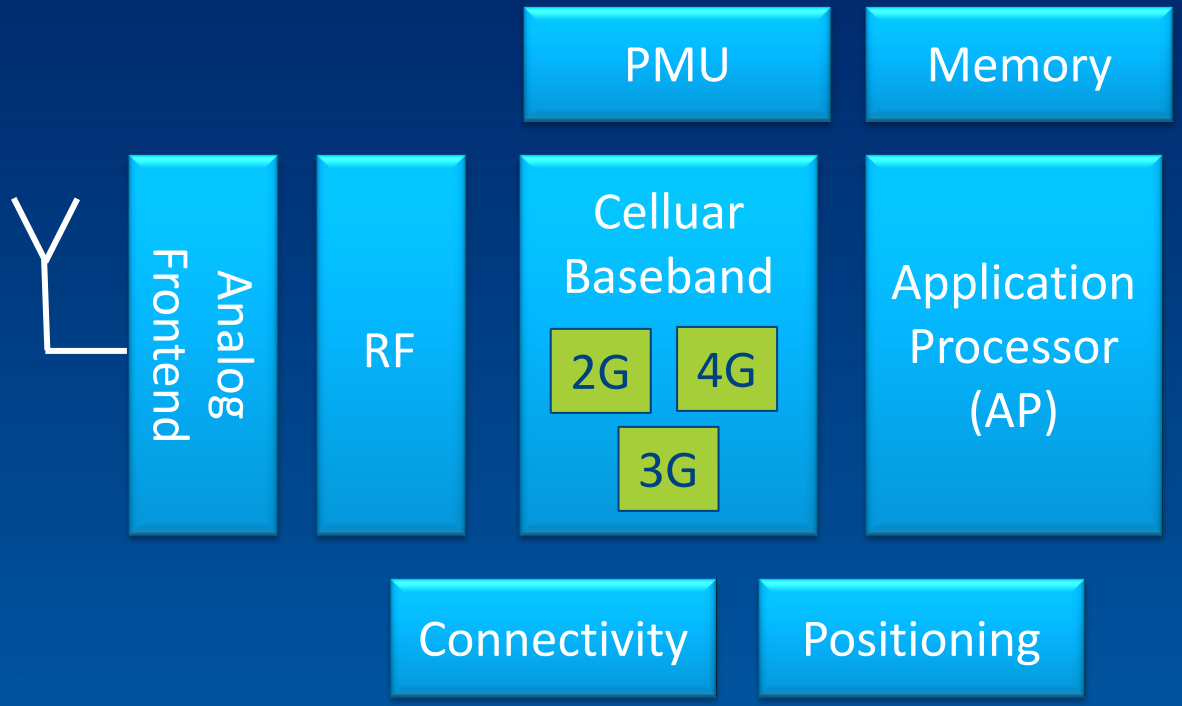
- Wireless SOCs
- Wireless Trends and their projection on Wireless SOCs design
- Wireless Base Band ICs
- Verification challenges in cellular devices
- Verification approaches

Mobile and Communications Group

Powering the next generation of smartphones, tablets, feature phones, and connected devices with leading-edge technologies

- Focus of MCG in Europe:
  - Slim Modem Platforms
  - Baseband / RF / Stack
  - Modem SOCs
- Main sites:
  - Munich, Duisburg, Nurnberg, Dresden, Aalborg, Sophia-Antipolis

Mobile Phone Platforms



- Cellular Baseband:
  - wireless signal processing
  - wireless protocol stack

Key Challenges for Wireless SOCs

- Provide wanted functionality correctly and in time
- Provide best in class performance
- Provide best in class power consumption
- Povide lowest PCB area
- Enable lowest overall production cost

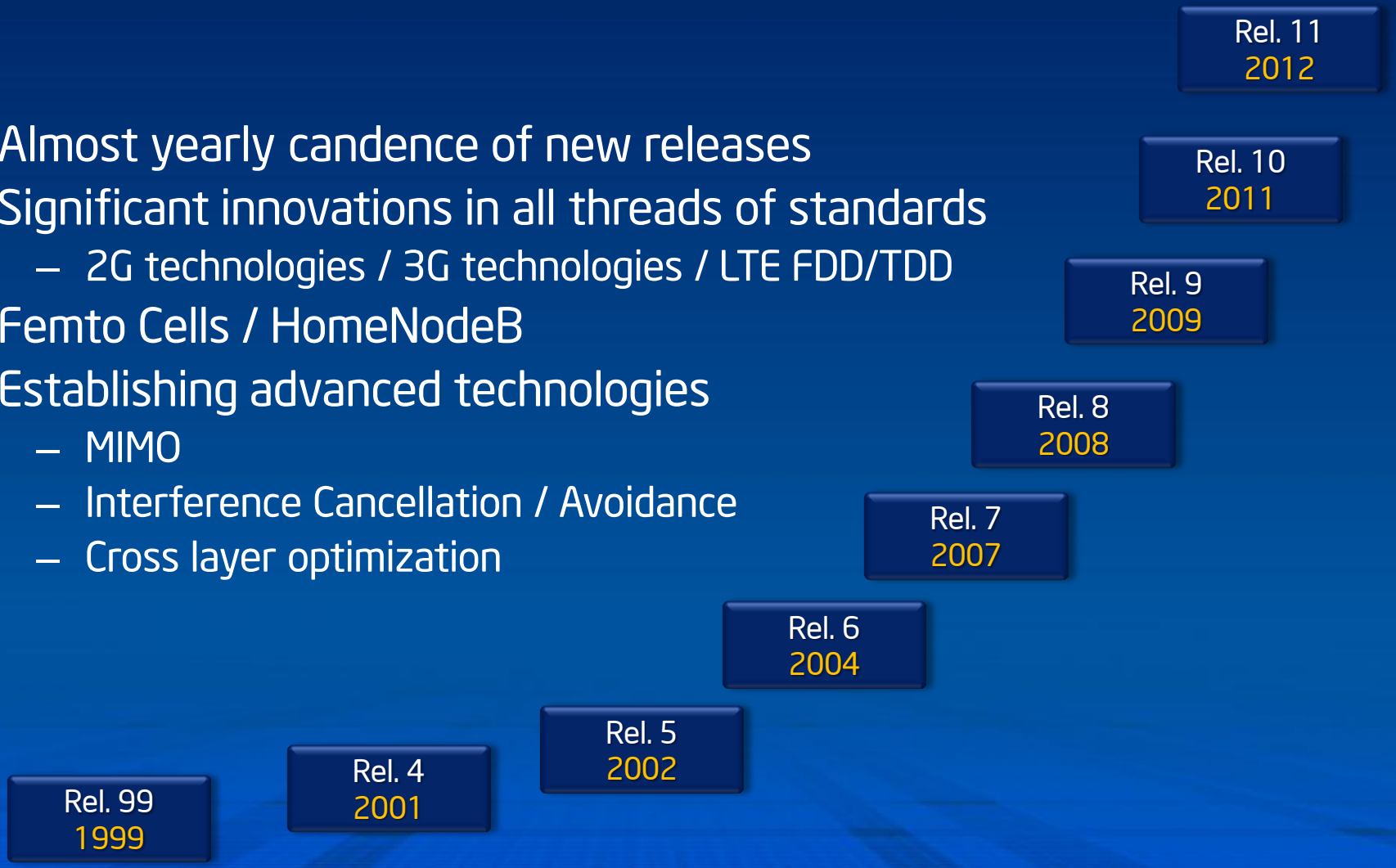
CURRENT TRENDS IN WIRELESS

Global Wireless Trends

- Europe:
  - Mature + well developed markets following general 3GPP trends
  - Comparably homegenous and sufficient sprectrum allocation
  - Little diversitifaction of operators wrt. radio access technologies (RATs)
- US:
  - Scarce + heterogeneous spectrum allocation: Carrier aggregation!
  - Radio Access Technologie is used as marketing argument
- ASIA:
  - Local RAT technologies (TD-SCDMa, LTE-TDD)
  - Multi-SIM operation

Standardisation

- Almost yearly candence of new releases
- Significant innovations in all threads of standards
  - 2G technologies / 3G technologies / LTE FDD/TDD
- Femto Cells / HomeNodeB
- Establishing advanced technologies
  - MIMO
  - Interference Cancellation / Avoidance
  - Cross layer optimization



Implications on BB technology

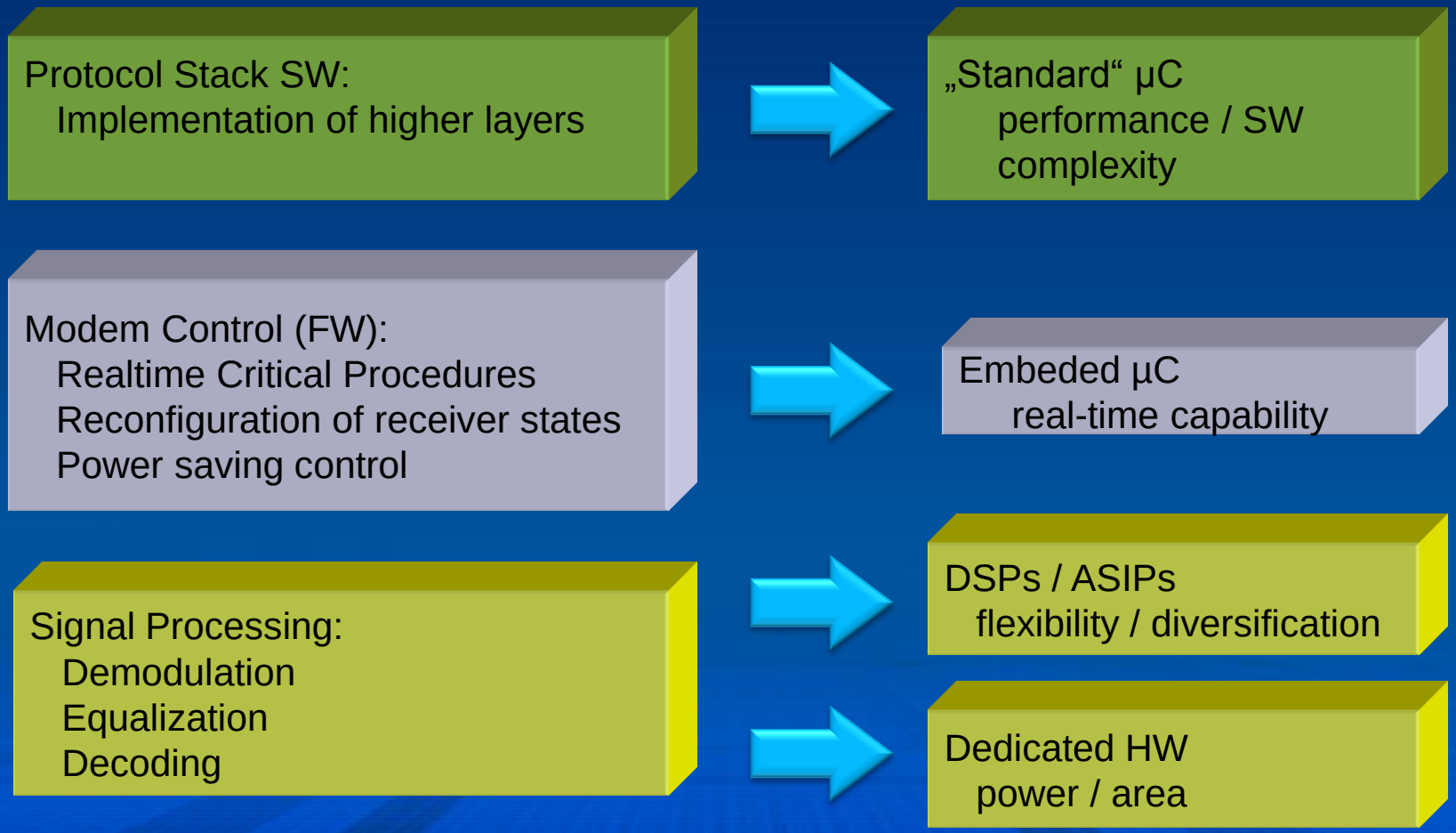
- Need to squeeze more and more different RATs into one platform
- Multi-SIM / Multi-Play limits ressource reuse
- Advanced signal-processing is mandatory and requires excessive aditional processing ressources
- „Shannon still beats Moore“
- Control flow / dynamic reconfiguration will even further increases
- SOC integration will become standard within a few years

- Dedicated data-path based architectures are still the best choice
- SW / FW complexity will futher increase

BB ARCHITECTURES & VERIFICATION

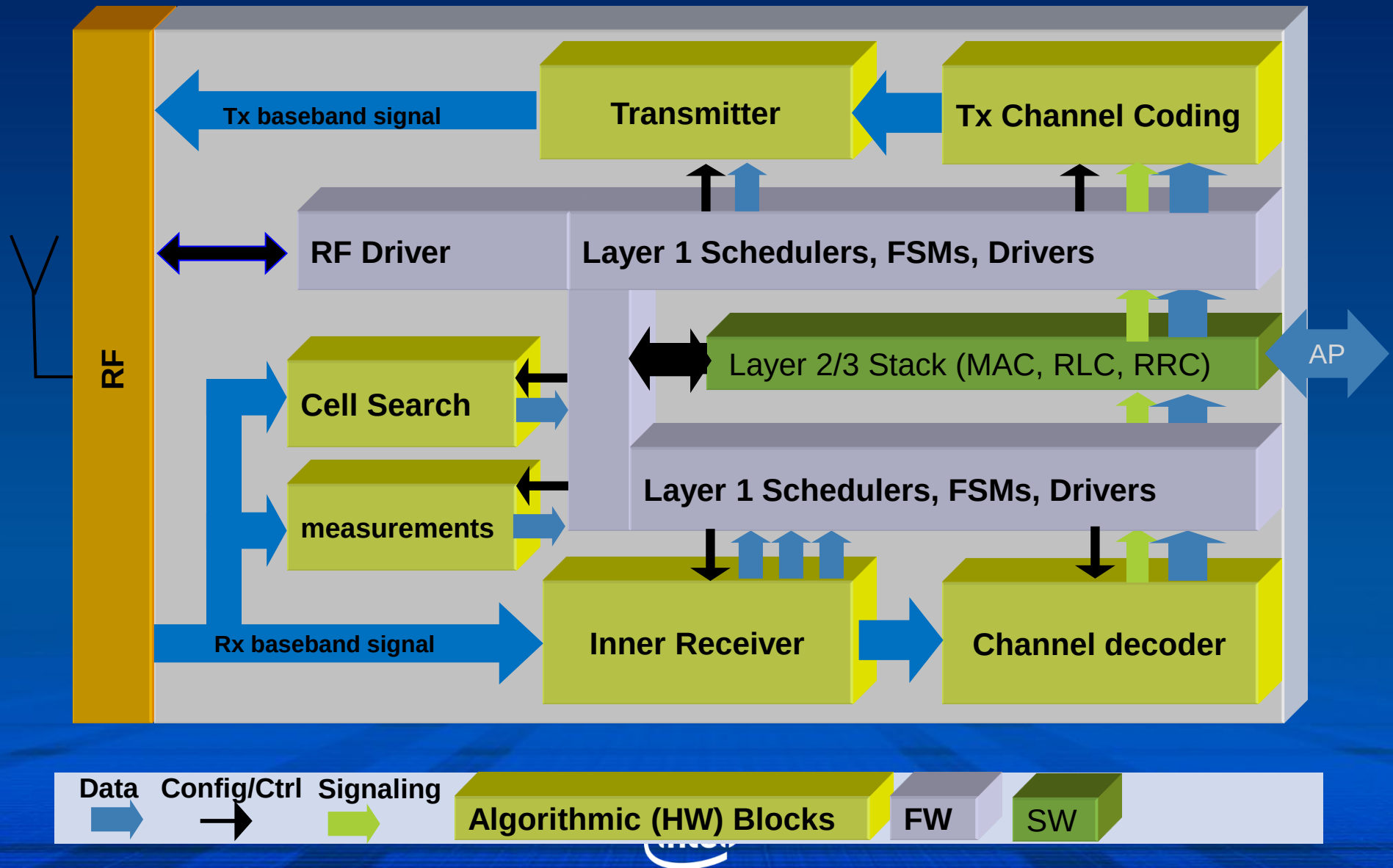
Wireless L1 Baseband Modem

architecture elements

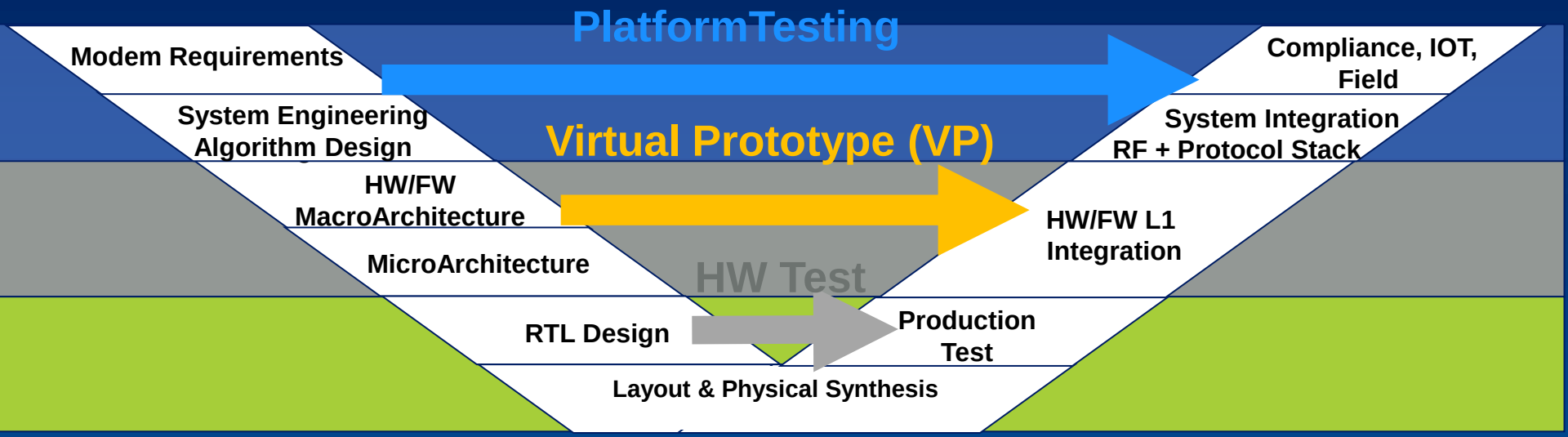


Wireless L1 Baseband Modem

general architecture



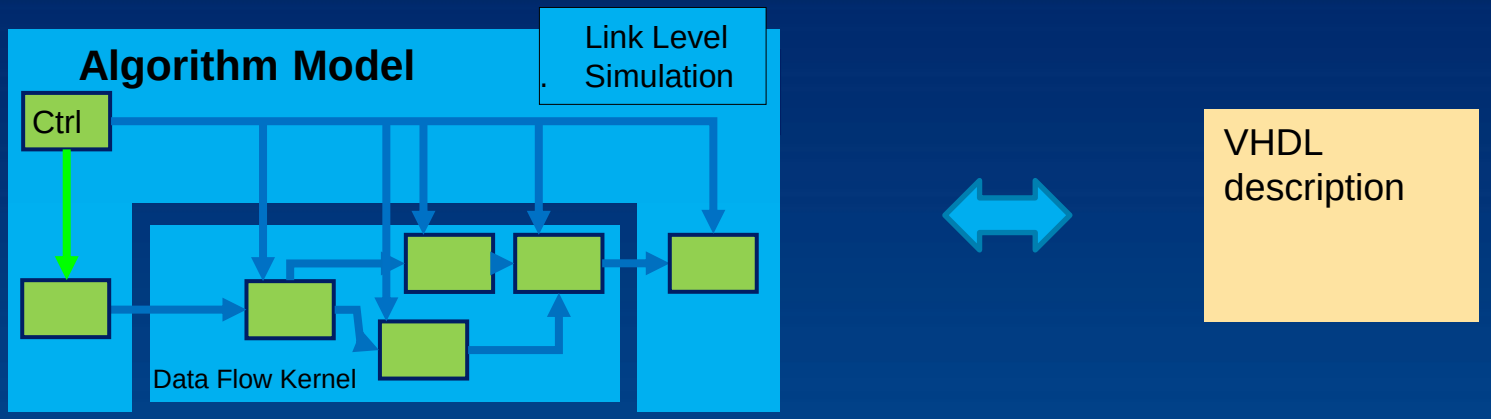
The V Model and the Virtual Prototype



- Detect errors as early in time as possible
  - Long time before silicon availablity!
- Algorithm simulation -> test statistical performance against 3GPP requirements
- HW simulation -> test HW implementation against specificatio

Pre silicon test system behavior / FW?
-> Virtual Prototype

HW Verification

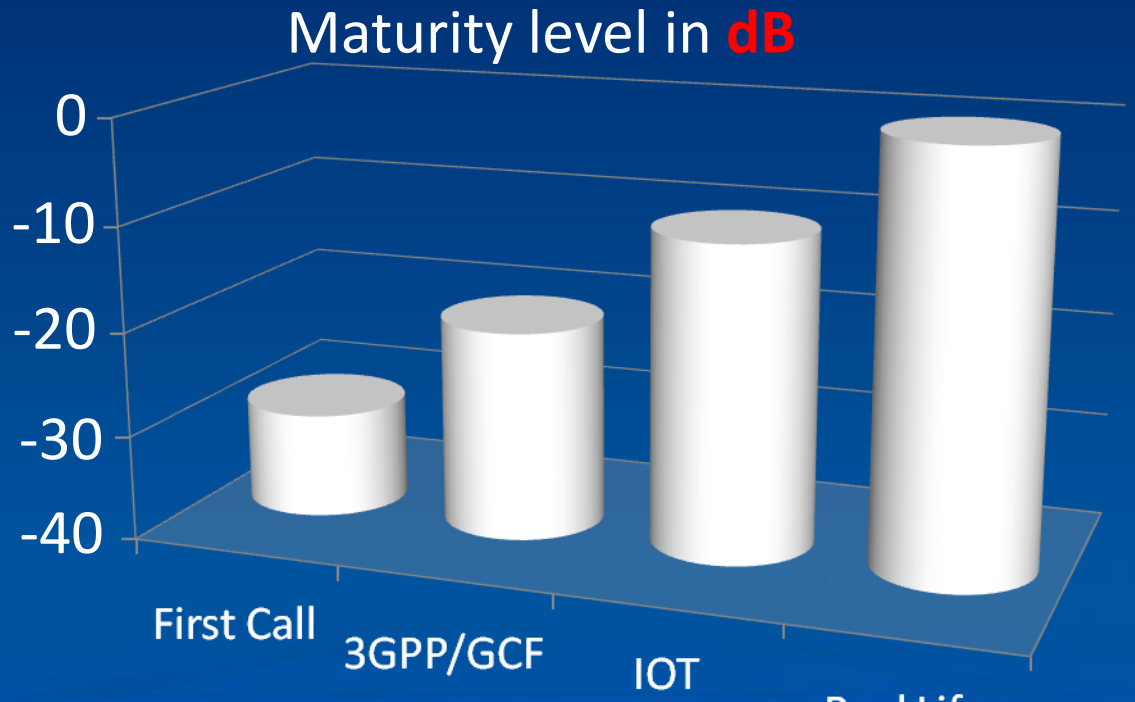


- Hierarchical verification
- Limited / controllable number of use cases
- HW Block level: exhaustive tests
- HW system level: test of typical + corner-case scenarios

- a few thousand Test Cases will give you a very good coverage
- very mature technology

Verification Challenge of Mobile Phone Platforms

Development of the maturity of the platform during bring-up



First Call: Simple stationary call against tester or live network
GCF: Global Certification Forum („3GPP standard compliance")
IOT: Inter Operability Testing (Compliance to network vendors and operators)
Real Life: Field Testing, Customer Testing, Operator Approval Testing (AT&T ADAPT, DoCoMo!)

Verification Challenge of Mobile Phone Platforms

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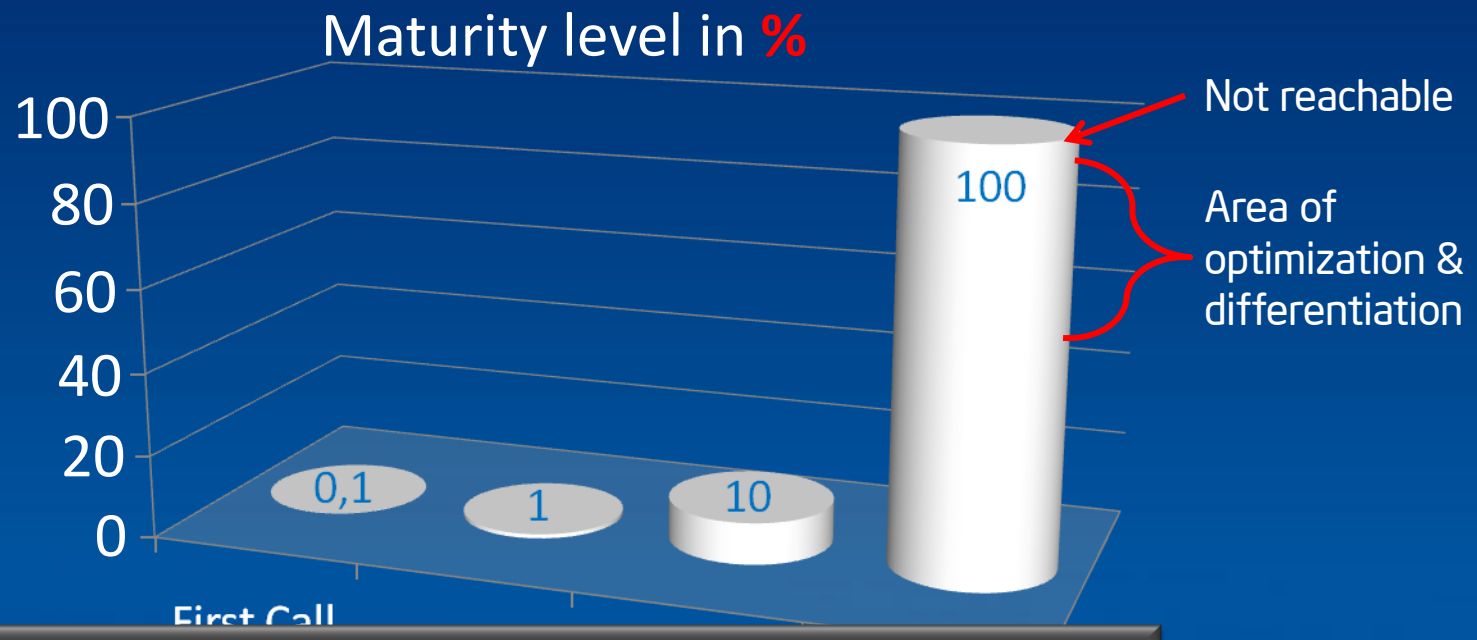
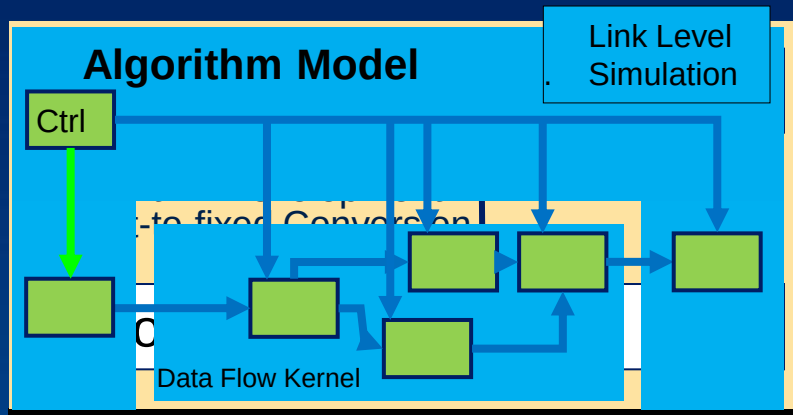


Link level simulation + HW Verification will cover less than 5% of the product functionality

First Call: Simple
GCF: Global Certi
IOT: Inter Operab
Real Life: Field Testing, Customer Testing, Operator Approval Testing (AT&T ADAPT, DoCoMo!)

intel

From <5% to 100% L1 product functionality

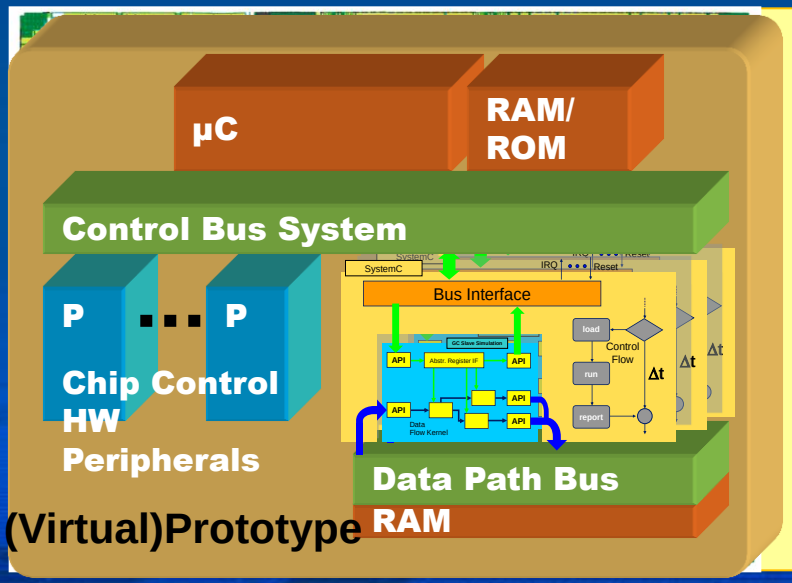


Properties:
Meets 3GPP Layer 1 Compliance Tests
algorithmic tracking
performance requirements

< 5% of L1 product functionality

How to get there?

Virtual Prototye
Thousands of TC



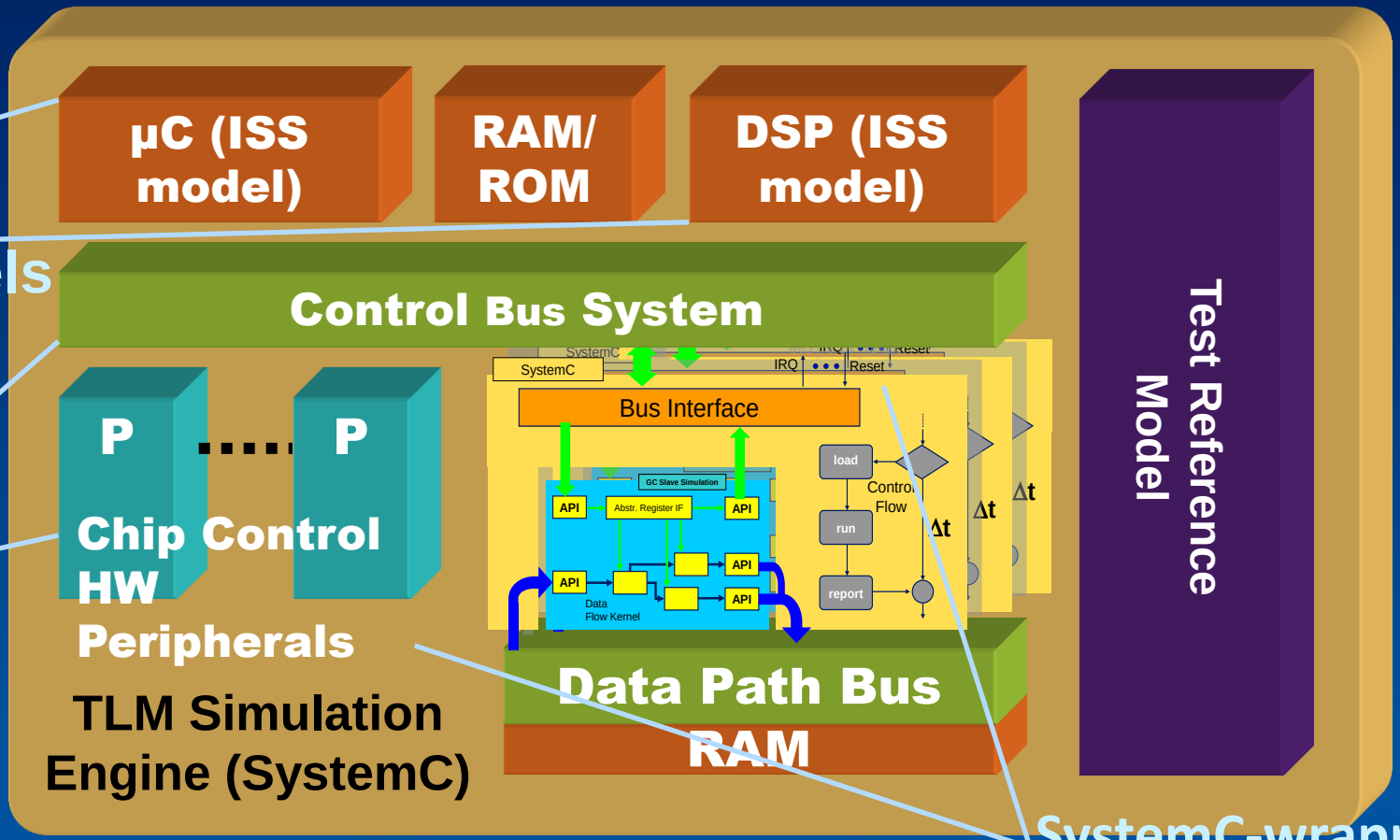
Executable Specification

100% L1 product functionality

- physical layer procedures
- dynamic PHY reconfigurations
- flexible HW/FW Interaction
- adaptive modulation & coding
- acquisition & tracking
- wakeup / sleep
- call setup / paging

Early HW/SW Integration
System Verification

Complete VP & Test System



3rd party ISS models

SystemC Models

SystemC-wrapped algorithmic reference model (C/C++)

System Level Reference

- Commercial test equipment is limited to 3GPP tests
- Hand-coded complex use-cases
- Require detailed knowledge about 3GPP specification
- Require detailed knowledge about implementation / corner-cases
- Are still very limited with respect to coverage of real scenarios

The VP is „just“ an executable Spec of the HW Model
We need an executable spec of the System Behavior!

EXAMPLE: 3GPP CPC DTX/DRX MODE

3GPP CPC feature

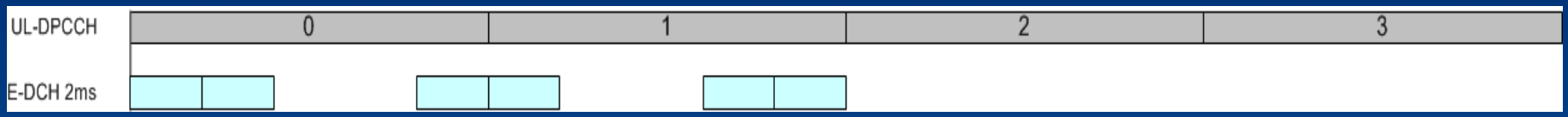
- Intention:
  - Replace CS Rel.99 voice technology by HSDPA
  - Move from continuous 3G transmission to a more burst-wise pattern
  - Power saving
  - Significantly Increased cell capacity
- Introduced in Rel.7 of 3GPP specification (2007)

Sounds cool

So why isn't it yet deployed in networks?

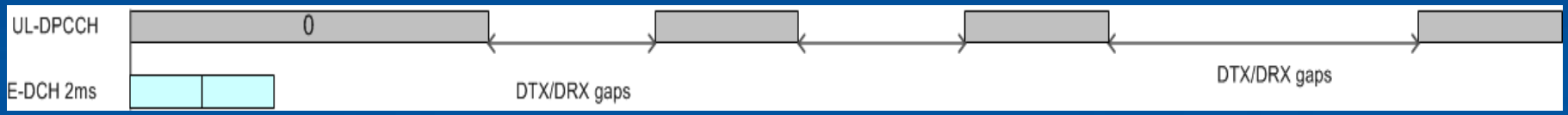
3GPP CPC principle

Continuous transmission



- Continuous RF transmission even if no data is transmitted / received
  - Impact on power consumption
  - Inefficient use of bandwidth / interference

CPC transmission



- Introduction of „smart" gap pattern if no data is transmitted / received
  - Keep activity to the minimum needed for L1 procedures
  - Variable pattern to maximise „silent" periods
  - Activity sensing

CPC DTX parameters

Parameter	Function
UE DTX cycle 1	DPCCH activity pattern, when UE DTX cycle 1 is active
UE DTX cycle 2	DPCCH activity pattern when UE DTX cycle 2 is active
UE DPCCH burst 1	Length of DPCCH transmission when UE DTX cycle 1 is active
UE DPCCH burst 2	Length of DPCCH transmission when UE DTX cycle 2 is active
Inactivity Threshold for UE DTX cycle 2	Activation of UE DTX cycle 2 after the last uplink data transmission
UE DTX long preamble length	Uplink preamble length
CQI DTX Timer	Priority period of the CQI reports after a HS-DSCH reception
Enabling Delay	Time-out period befor enabling DRX/DTX pattern
UE DTX DRX Offset	UE specific offset of DRX and DTX cycles

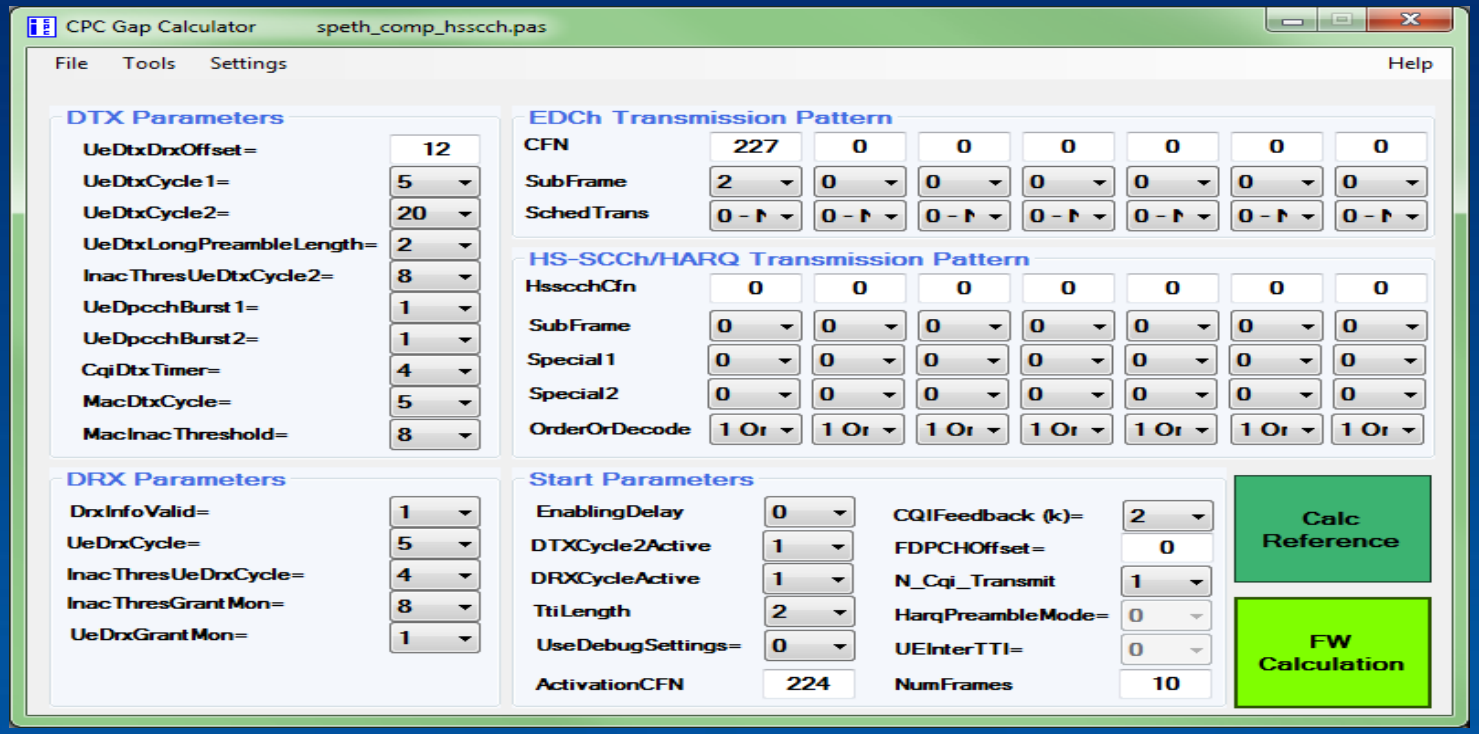
CPC DRX parameters

Parameter	Function
MAC DTX cycle	HS-SCCH reception pattern
MAC Inactivity Threshold	E-DCH inactivity time before MAC DTX cycle gets active
UE DRX cycle	Length of DPCCH transmission when UE DTX cycle 1 is active
Inactivity threshold for UE DRX cycle	Interval for HS-SCCH monitoring after downlink activity
Inactivity Threshold for UE Grant Monitoring	Interval for E-AGCH/E-RGCH monitoring after uplink activity
UE DRX Grant Monitoring	Corner case E-AGCH/E-RGCH monitoring
Enabling Delay	Time threshold before enabling new DRX/DTX pattern

- Looks not really killing but how to specify?

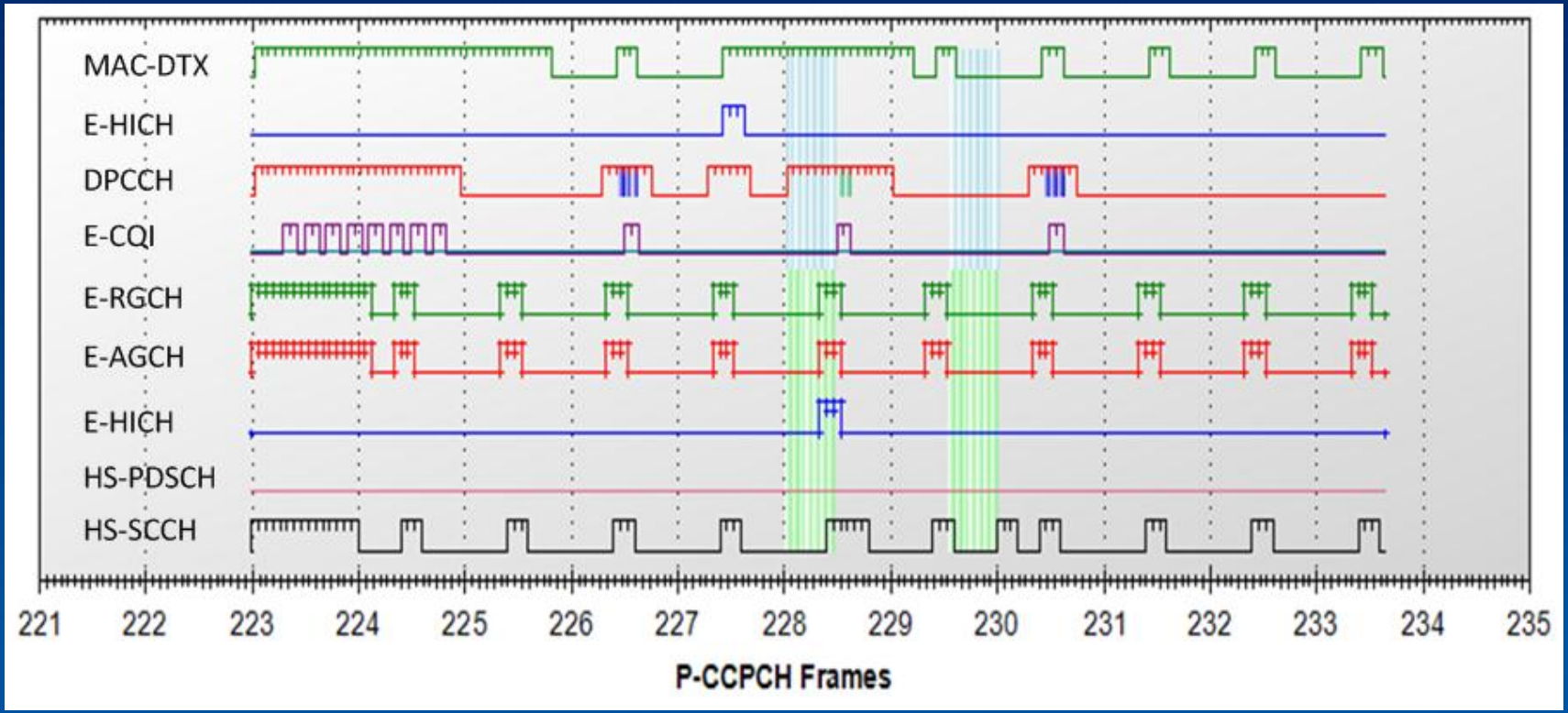
-> executable simulation / reference gap simulator

CPC gap calculator



Configuration Interface

CPC gap calculator



Example output

CPC gap-simulator

- Idea: Abstract model of DTX / DRX pattern
  - Discard any signal processing
  - Just simulate the activity pattern without any detail information
- Result:
  - Total simulator (including graphical frontend)
    ~ several 1000 lines of code
  - DTX / DRX functionality
    ~ several 100 lines of code

- Time-consuming + cumbersome even at this level of abstraction
- Real implementation is magnitudes more complex
- Still limited in functionality / use-cases

System Level Reference Model

3GPP specification:
~ 10 references in the standard
~ 16 parameters

CPC Gap simulator:
- hundreds of lines of code!
- missing abstraction

Is there a way of abstraction to complex system behavior?

- We need an executable system level spec
  - Abstraction, not a sample implementation
  - Use as little detail as possible
  - Model *really* complex scenarios:
    - Complete L1 behavior, not limited to data-path
    - Complex network topologies, not limited to single link
    - Complex use-cases: (soft) handover, InterRAT ...
    - Interaction with higher-layers ...

First approach: Timed stream driven simulation

- Use processing elements containing abstract attributes instead of physical channel samples
- Use causality / timing relations between physical channels to trigger activation of processing nodes
- Generate implicite scheduling via an adequate topology of processing nodes

Any hints concerning existing approaches, tools, scientific work welcome!

summary

- Given current wireless trends there is no paradigm change in wireless modems architectures to be expected
- Given the rapid development of standards the pressure on power consumption and minimizing area remains unchanged
- Verifying the complete system is the biggest challenge
- VPs are inevitable tools for system verification but they are only an executable spec for the HW Behavior
- We need a methodology / abstraction mechanisms for an executable specification for the System Behavior